UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,020	03/08/2001	Ashley Saulsbury	016747015210	4703

20350 7590 03/23/2004

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 03/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,020	SAULSBURY ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cov r she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment A, filed 2/4/2004.

2. Claims 1-18 and 20-22 are pending in this application. Claims 1, 9 and 17 are independent claims. In Amendment A, claims 1-2 and 17 are amended, claim 19 is cancelled, and claims 21-22 are added. This action is made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-18 and 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Sidwell et al. (U.S. 5,875,355).

Re claim 1, Sidwell et al. disclose in Figures 7, 10, and 15 a method for processing a matrix of elements in a processor (abstract discloses the processes of transposing the matrix), the method comprising steps of: loading a first subset of matrix elements from a first location (Annexe A Sequence (ii) in cols. 15-16 wherein Figure 10 illustrates the zip instruction as reading from SRC1 to 170 for first subset of matrix elements); loading a second subset of matrix elements from a second location (Annexe A Sequence (ii) in cols. 15-16 wherein Figure 10 illustrates the zip instruction as reading from SRC2 to 172 for second subset of matrix elements); storing a third subset of matrix

elements in a first destination (Annexe A Sequence (ii) in cols. 15-16 wherein Figure 10 illustrates the zip instruction as storing into 176 for first final transpose matrix as seen in Figure 15 bottom right matrix); and storing a fourth subset of matrix elements in a second destination (Annexe A Sequence (ii) in cols. 15-16 wherein Figure 10 illustrates the zip instruction as storing into 174 for second final transpose matrix as seen in Figure 15 bottom right matrix), wherein the loading and storing steps result from a first instruction issue (160 OPCODE and Zip Instruction of 192) at least one of the first and second destination consists of a row or column of a second matrix (Figure 15 bottom right matrix e.g. R1 = {A0 B0 C0 D0} is a transposed of {A0; B0; C0; D0}) and the second matrix corresponds to a transposition of the matrix (each row or register in Figure 15 bottom right matrix is an transposed vector of the original matrix upper left).

Re claim 2, Sidwell et al. further disclose a first number of sub-instructions perform a matrix transpose and the matrix transpose operates on the matrix that has a number of columns equal to the first number (n = 4 in the case and there are 4 instructions in Figure 15 in order to complete the transposition as recited in cols. 15-16 Annexe A Sequence (ii)).

Re claim 3, Sidewell et al. further disclose in Figure 10 the first loading step is performed with a first processing path (path SRC1 to 170) and the second loading step is performed with a second processing path (path SRC2 to 170).

Re claim 4, Sidewell et al. further disclose in Figures 10 and 15 comprising steps of: loading a first subset of matrix elements from a fifth location; loading a sixth subset of matrix elements from a sixth location; storing a seventh subset of matrix elements in a

third destination; and storing eighth subset of matrix elements in a fourth destination (these instruction is further processes another subset of matrix e.g. 3rd and 4th rows).

Re claim 5, Sidewell et al. further disclose in Figure 15 the loading and storing steps introduced result from a second instruction issue (Zip interleaved rows of 32 bit objects or flips instruction).

Re claim 6, Sidewell et al. further disclose in Figure 15 each of the first through fourth destination includes a matrix column (any elements in the table).

Re claim 7, Sidewell et al. further disclose in Figure 15 each the first through fourth locations include a matrix row (any elements in the table).

Re claim 8, Sidewell et al. further disclose in Figures 7 and 15 the third and fourth subsets each comprise elements from the first and second subsets (3rd table of Figure 15).

Re claim 9, it is a processing claim of claim 3. Thus, claim 9 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 10, Sidewell et al. further disclose in Figure 10 the 1st through 4th registers each include a plurality of source fields, and each source field includes a matrix element (S1[X] and S2[X]).

Re claim 11, Sidewell et al. further disclose in Figure 10 the 1st and 2nd destination registers each include a plurality of result fields and each source field includes a matrix element (174 and 176).

Re claim 12, Sidewell et al. further disclose in Figure 10 wherein 1st and 2nd instruction processors; and an exchange path between the first and second instruction processors (180, 182, 184, 186, 188, and 190).

Re claim 13, Sidewell et al. further disclose in Figure 10 the 1st processing path receives a 1st sub-instruction and the 2nd processing path receives a 2nd sub-instruction (output from 192 that goes into 180, 182, 184, 186, 188, and 190).

Re claim 14, it is a processing claim of claim 7. Thus, claim 14 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 15, it is a processing claim of claim 6. Thus, claim 15 is also rejected under the same rationale in the rejection of rejected claim 6.

Re claim 16, Sidewell et al. further disclose in Figures 7-8, 10, and 15 the 1st and 2nd destination registers are addressed by a 1st and 2nd sub-instructions which are included in a VLIW (Zip, Unzip, Flip instruction).

Re claim 17, it is a method claim of claim 3. Thus, claim 17 is also rejected under the same rationale in the rejection of rejected claim 3 (Figure 15 and cols. 15-16 Annexe A Sequence (ii)).

Re claims 18-19, Sidewell et al. further disclose in Figures 10 and 12 the 1st and 2nd instructions include a first operation code and the third and fourth instructions include a second operation code different from the first operation code (160 in Figure 10 and 160 in Figure 12).

Re claim 20, it is a method claim of claim 16. Thus, claim 20 is also rejected under the same rationale in the rejection of rejected claim 16.

Response to Arguments

5. Applicant's arguments filed 2/4/2004 have been fully considered but they are not persuasive.

a. The applicant argues in page 11 for claim 1 that the cited reference does not disclose that the destination has only a single row or column from the transposed matrix.

The examiner respectfully submits that the claim language does not implicitly require the destination register has only either a single row or column from the transposed matrix. In addition, the cited reference clearly discloses that the final destination registers in row contains a column of the transposed matrix (e.g. R1 = {A0 B0 C0 D0} is a transposed of {A0; B0; C0; D0}).

b. The applicant argues in page 12 for claim 9 that the cited reference does not disclose coupling a first processing path to the first through fourth source registers.

The examiner respectfully submits that base on the claim language, it does not require all first through fourth sources registers operates in parallel or instantaneous. Rather, the claim language only requires a first processing path coupling (e.g. connect) to the first through fourth source registers, which can be seen in Annexe A Sequence (ii) the first two zip instructions involve all four registers R1-R4.

c. The applicant argues in page 12 for claim 17 that the cited reference does not disclose having four sub-instructions in the same issue.

The examiner respectfully submits that the cited reference clearly discloses in cols. 15-16 Annex A Sequence (ii) four same sub-instructions zip2n4v2p that operates on the same matrix elements.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

March 15, 2004

TODD INGBERG
PRIMARY EXAMINER